Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70427

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering and Robotics and Automation Engineering)

(Regulations 2013)

(Also Common to PTEC 6302 – Digital Electronics for B.E. (Part-Time) Second Semester – Electronics and Communication Engineering – (Regulations – 2014))

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Prove the Boolean theorems :

   (a) $x + x = x$

   (b) $x + xy = x$

2. Define Noise margin.

3. Draw the truth table and the logic circuit of half adder.

4. Compare the function of Decoder and Encoder.

5. What are the classifications of sequential circuits?

6. What is edge-triggered flip-flop?

7. Briefly explain about EEPROM.

8. What is programmable logic array? How it differs from ROM?

9. Distinguish between a combinational logic circuit and a sequential logic circuit.

10. What is the most important consideration in making state assignments for asynchronous network?

PART B — (5 × 13 = 65 marks)

11. (a) Simplify the following Boolean function F, using Quine Mccluskey method and verify the result using K-map F(A, B, C, D) = Σ (0, 2, 3, 5, 7, 9, 11, 13, 14). (13)

Or

(b) (i) Draw and explain Tri-state TTL inverter circuit diagram with its operation. (8)

(ii) Implement the following function using NAND and inverter gates. (5)

$$F = AB + A'B' + B'C$$

12. (a) (i) Design and explain 1 of 8 demultiplexer. (8)

(ii) What is parity checker? (5)

Or

(b) Describe the operation of 3-bit magnitude comparator. (13)

13. (a) Using D flipflops design a synchronous counter which counts in the sequence. 000, 001, 010, 011, 100, 101, 110, 111, 000. (13)

Or

(b) (i) Discuss the working of a 4 bit Johnson counter with neat block diagram. (7)

(ii) Explain the functioning of a recirculating shift register with various modes of operation. (6)

14. (a) Write the differences between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. (13)

Or

(b) Write notes on :

(i) PAL (7)

(ii) FPGA. (6)

15. (a) (i) Summarize the design procedure for a synchronous sequential circuit. (10)

(ii) Derive the state table of a serial binary adder. (3)

Or

(b) What is the objective of state assignment in a asynchronous circuit? Give the hazard free realization for the Boolean function f (A, B, C, D) = M (0, 2, 6, 7, 8, 10, 12). (13)

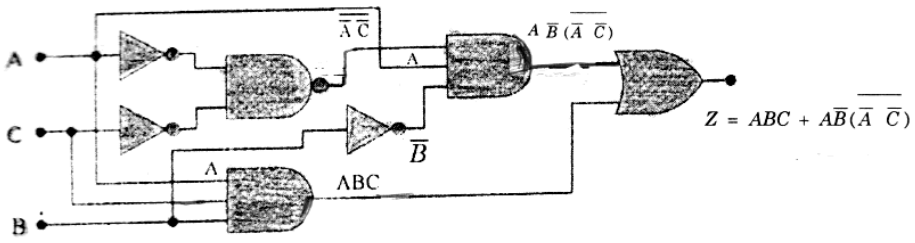
PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a circuit that has a 3-bit binary input and a single output (Z) specified as follows : (8)

Z = 0, when the input is less than 5_{10}

Z = 1, otherwise

(ii) Simplify the given logic circuit using Boolean Simplification. (7)



Or

(b) Design a synchronous sequential circuit whose state diagram is shown below. (15)